# DEPARTMENT OF ECE

## MICROPROCESSSOR AND MICROCONTROLLER

1. The register that may be used as an operand register is
a) Accumulator
b) B register
c) Data register
d) Accumulator and B register

2. The register that can be used as a scratch pad is
a) Accumulator
b) B register
c) Data register
d) Accumulator and B register

3. The registers that contains the status information is
a) control registers
b) instruction registers
c) program status word
d) all of the mentioned

4. Which of the processor's stack does not contain the top-down data structure?
a) 8086
b) 80286
c) 8051
d) 80386

5. The architecture of 8051 consists of
a) 4 latches
b) 2 timer registers
c) 4 on-chip I/O ports
d) all of the mentioned

6. The transmit buffer of serial data buffer is a
a) serial-in parallel-out register
b) parallel-in serial-out register
c) serial-in serial-out register

d) parallel-in parallel-out register

7. The receive buffer of serial data buffer is a
a) serial-in parallel-out register
b) parallel-in serial-out register
c) serial-in serial-out register
d) parallel-in parallel-out register

8. The register that provides control and status information about counters is
a) IP
b) TMOD
c) TSCON
d) PCON

9. The register that provides control and status information about serial port is
a) IP
b) IE
c) TSCON
d) PCON and SCON

10. The device that generates the basic timing clock signal for the operation of the circuit using crystal oscillator is
a) timing unit
b) timing and control unit
c) oscillator
d) clock generator

11. The registers that are not accessible by the user are
a) Accumulator and B register
b) IP and IE
c) instruction registers
d) TMP1 and TMP2

12. Which of the following is an 8-bit register?
a) PSW(Program Status Word)
b) TCON(Timer Control Register)
c) Accumulator

d) all of the mentioned

13. Which of the following register can be addressed as byte?
a) P1
b) SCON
c) TMOD
d) TCON

14. Which of the following is bit-addressable register?
a) SBUF
b) PCON
c) TMOD
d) SCON

15. The higher and lower bytes of a 16-bit register DPTR are represented respectively as
a) LDPTR and HDPTR
b) DPTRL and DPTRH
c) DPH and DPL
d) HDP and LDP

16. The register that is used for accessing external data memory is
a) DPH
b) DPL
c) DPTR
d) NONE

17. Among the four groups of register banks, the number of groups that can be accessed at a time is
a) 1
b) 2
c) 3
d) all the four.

18. The number of 8-bit registers that a register bank contain is
a) 2
b) 4
c) 6
d) 8

19. If RS1=1, RS0=0, then the register bank selected is
a) register bank 0
b) register bank 1
c) register bank 2
d) register bank 3

20. If RS1=1, RS0=1, then the register bank selected is
a) register bank 0
b) register bank 1
c) register bank 2
d) register bank 3

21. The PCON register consists of
a) power mode bit
b) power idle bit
c) power ideal bit
d) power down bit and idle bit

22. The on-chip oscillator is stopped in
a) power mode
b) power down mode
c) idle mode
d) ideal mode

23. In idle mode, the device that is disabled is
a) serial port
b) timer block
c) clock to CPU
d) all of the mentioned

24. The only way to terminate the power down mode is to
a) CLEAR
b) RESET
c) HOLD
d) HLT

25. The idle mode can be terminated by
a) PRESET

b) CLEAR
c) interrupt
d) interrupt or reset

26. Which of the following is an external interrupt?
a) INT0(active low)
b) INT2(active low)
c) Timer0 interrupt
d) Timer1 interrupt

27. The interrupts, INT0(active low) and INT1(active low) are processed internally by flags
a) IE0 and IE1
b) IE0 and IF1
c) IF0 and IE1
d) IF0 and IF1

28. The flags IE0 and IE1, are automatically cleared after the control is transferred to respective vector, if the interrupt is
a) level-sensitive
b) edge-sensitive
c) in serial port
d) in parallel port

29. If the external interrupt sources control the flags IE0 and IE1, then the interrupt programmed is
a) level-sensitive
b) edge-sensitive
c) in serial port
d) in parallel port

30. The pulses at T0 or T1 pin are counted in
a) timer mode
b) counter mode
c) idle mode
d) power down mode

31. In timer mode, the oscillator clock is divided by a prescalar
a) (1/8)
b) (1/4)

c) (1/16)
d) (1/32)

32. The serial port interrupt is generated if
a) RI is set
b) RI and TI are set
c) either RI or TI is set
d) RI and TI are reset

33. In serial port interrupt, after the control is transferred to the interrupt service routine, the flag that is cleared is
a) RI
b) TI
c) RI and TI
d) none

34. The atleast number of machine cycles for which the external interrupts that are programmed level-sensitive should remain high is
a) 1
b) 2
c) 3
d) 0

35. If the external interrupts are programmed edge sensitive, then they should remain high for atleast
a) 0 machine cycle
b) 2 machine cycles
c) 1 machine cycle
d) 3 machine cycles

36. The timer generates an interrupt, if the count value reaches to
a) 00FFH
b) FF00H
c) 0FFFH
d) FFFFH

37. The external interrupt that has the lowest priority among the following is
a) TF0
b) TF1

c) IE1
d) NONE

38. Among the five interrupts generated by 8051, the lowest priority is given to the interrupt
a) IE0
b) TF1
c) TF0
d) RI

39. Among the five interrupts generated by 8051, the highest priority is given to the interrupt
a) IE0
b) TF1
c) TF0
d) IE1

40. All the interrupts are enabled using a special function register called
a) interrupt priority register
b) interrupt register
c) interrupt function register
d) interrupt enable register

41. The number of bytes stored on the stack during one operation of PUSH or POP is
a) 1
b) 2
c) 3
d) 4

42. The step involved in PUSH operation is
a) increment stack by 2 and store 8-bit content to address pointed to by SP
b) decrement stack by 1 and store 16-bit content to address pointed to by SP
c) increment stack by 1 and store 8-bit content to address pointed to by SP
d) store 8-bit content to address pointed to by SP and then increment stack by 1

43. Once the processor responds to an INTR signal, the IF is automatically
a) set
b) reset
c) high
d) low

44. The step involved in POP operation is
a) decrement stack by 2 and store 8-bit content to address pointed to by SP
b) store 16-bit content to address pointed to by SP and decrement stack by 1
c) decrement stack by 1 and store content of top of stack to address pointed to by SP
d) store content of top of stack to address pointed to by SP and then decrement stack by 1

45. The 8051 stack is
a) auto-decrement during PUSH operations
b) auto-increment during POP operations
c) auto-decrement during POP operations
d) auto-increment during PUSH operations

46. After reset, the stack pointer(SP) is initialised to the address of
a) internal ROM
b) internal RAM
c) external ROM
d) external RAM

47. Which of the following is not an addressing mode of 8051?
a) register instructions
b) register specific instructions
c) indexed addressing
d) none

48. The symbol, ‘addr 16’ represents the 16-bit address which is used by the instructions to specify the
a) destination address of CALL
b) source address of JUMP
c) destination address of call or jump
d) source address of call or jump

49. The storage of addresses that can be directly accessed is
a) external data RAM
b) internal data ROM
c) internal data RAM and SFRS
d) external data ROM and SFRS

50. The address register for storing the 16-bit addresses can only be
a) stack pointer

b) data pointer
c) instruction register
d) accumulator

51. The address register for storing the 8-bit addresses can be
a) R0 of selected bank of register
b) R1 of selected bank of register
c) stack pointer
d) all of the mentioned

52. The instruction, ADD A, R7 is an example of
a) register instructions
b) register specific instructions
c) indexed addressing
d) none

53. The addressing mode, in which the instructions has no source and destination operands is
a) register instructions
b) register specific instructions
c) direct addressing
d) indirect addressing

54. The instruction, RLA performs
a) rotation of address register to left
b) rotation of accumulator to left
c) rotation of address register to right
d) rotation of accumulator to right

55. The instruction, ADD A, #100 performs
a) 100(decimal) is added to contents of address register
b) 100(decimal) is subtracted from accumulator
c) 100(decimal) is added to contents of accumulator
d) none

56. In which of these addressing modes, a constant is specified in the instruction, after the opcode byte?
a) register instructions
b) register specific instructions
c) direct addressing

d) immediate mode

57. The only memory which can be accessed using indexed addressing mode is
a) RAM
b) ROM
c) main memory
d) program memory

58. The data address of look-up table is found by adding the contents of
a) accumulator with that of program counter
b) accumulator with that of program counter or data pointer
c) data register with that of program counter or accumulator
d) data register with that of program counter or data pointer

59. The instruction, MOV AX, 0005H belongs to the address mode
a) register
b) direct
c) immediate
d) register relative

60. The instruction, MOV AX, 1234H is an example of
a) register addressing mode
b) direct addressing mode
c) immediate addressing mode
d) based indexed addressing mode

61. The instruction, MOV AX, [2500H] is an example of
a) immediate addressing mode
b) direct addressing mode
c) indirect addressing mode
d) register addressing mode

62. If the data is present in a register and it is referred using the particular register, then it is
a) direct addressing mode
b) register addressing mode
c) indexed addressing mode
d) immediate addressing mode

63. The instruction, MOV AX,[BX] is an example of
a) direct addressing mode
b) register addressing mode
c) register relative addressing mode
d) register indirect addressing mode

64. If the offset of the operand is stored in one of the index registers, then it is
a) based indexed addressing mode
b) relative based indexed addressing mode
c) indexed addressing mode
d) none of the mentioned

65. The addressing mode that is used in unconditional branch instructions is
a) intrasegment direct addressing mode
b) intrasegment indirect addressing mode
c) intrasegment direct and indirect addressing mode
d) intersegment direct addressing mode

66. If the location to which the control is to be transferred lies in a different segment other than the current one, then the mode is called
a) intrasegment mode
b) intersegment direct mode
c) intersegment indirect mode
d) intersegment direct and indirect mode

67. The instruction, JMP 5000H:2000H;
is an example of
a) intrasegment direct mode
b) intrasegment indirect mode
c) intersegment direct mode
d) intersegment indirect mode

68. The contents of a base register are added to the contents of index register in
a) indexed addressing mode
b) based indexed addressing mode
c) relative based indexed addressing mode
d) based indexed and relative based indexed addressing mode

69. The instruction that is used to transfer the data from source operand to destination operand is
a) data copy/transfer instruction
b) branch instruction
c) arithmetic/logical instruction
d) string instruction

70. The instructions that involve various string manipulation operations are
a) branch instructions
b) flag manipulation instructions
c) shift and rotate instructions
d) string instructions

71. Which of the following instruction is not valid?
a) MOV AX, BX
b) MOV DS, 5000H
c) MOV AX, 5000H
d) PUSH AX

72. In PUSH instruction, after each execution of the instruction, the stack pointer is
a) incremented by 1
b) decremented by 1
c) incremented by 2
d) decremented by 2

73. The instruction that pushes the contents of the specified register/memory location on to the stack is
a) PUSHF
b) POPF
c) PUSH
d) POP

74. In POP instruction, after each execution of the instruction, the stack pointer is
a) incremented by 1
b) decremented by 1
c) incremented by 2
d) decremented by 2

75. The instructions that are used for reading an input port and writing an output port respectively are
a) MOV, XCHG

b) MOV, IN
c) IN, MOV
d) IN, OUT

76. The instruction that is used for finding out the codes in case of code conversion problems is
a) XCHG
b) XLAT
c) XOR
d) JCXZ

77. The instruction that loads effective address formed by destination operand into the specified source register is
a) LEA
b) LDS
c) LES
d) LAHF

78. The instruction that loads the AH register with the lower byte of the flag register is
a) SAHF
b) AH
c) LAHF
d) PUSHF

79. The instruction that pushes the flag register on to the stack is
a) PUSH
b) POP
c) PUSHF
d) POPF

80. The instruction that loads the flag register completely from the word contents of the memory location is
a) PUSH
b) POP
c) PUSHF
d) POPF

81. The instruction that adds immediate data/contents of memory location specified in an instruction/register to the contents of another register/memory location is

a) SUB
b) ADD
c) MUL
d) DIV

82. The instruction that supports addition when carry exists is
a) ADD
b) ADC
c) ADD & ADC
d) none of the mentioned

83. The assembler directives which are the hints using some predefined alphabetical strings are given to
a) processor
b) memory
c) assembler
d) processor & assembler

84. The directive used to inform the assembler, the names of the logicals segments to be assumed for different segments used in the program is
a) ASSUME
b) SEGMENT
c) SHORT
d) DB

85. Match the following

a) DB 1) used to direct the assembler to reserve only 10-bytes

b) DT 2) used to direct the assembler to reserve only 4 words

c) DW 3) used to direct the assembler to reserve byte or bytes

d) DQ 4) used to direct the assembler to reserve words

a) a-3,b-2,c-4,d-1
b) a-2,b-3,c-1,d-4
c) a-3,b-1,c-2,d-4
d) a-3,b-1,c-4,d-2

86. The directive that marks the end of an assembly language program is

a) ENDS
b) END
c) ENDS & END
d) None of the mentioned

87. The directive that marks the end of a logical segment is
a) ENDS
b) END
c) ENDS & END
d) None of the mentioned

88. The directive that updates the location counter to the next even address while executing a series of instructions is
a) EVN
b) EVEN
c) EVNE
d) EQU

89. The directive that directs the assembler to start the memory allotment for a particular segment/block/code from the declared address is
a) OFFSET
b) LABEL
c) ORG
d) GROUP

90. The directive that marks the starting of the logical segment is
a) SEG
b) SEGMENT
c) SEG & SEGMENT
d) PROC

91. The recurrence of the numerical values or constants in a program code is reduced by
a) ASSUME
b) LOCAL
c) LABEL
d) EQU

92. A machine language instruction format consists of

a) Operand field
b) Operation code field
c) Operation code field & operand field
d) none of the mentioned

93. The length of the one-byte instruction is
a) 2 bytes
b) 1 byte
c) 3 bytes
d) 4 bytes

94. The instruction format ‘register to register’ has a length of
a) 2 bytes
b) 1 byte
c) 3 bytes
d) 4 bytes

95. The R/M field in a machine instruction format specifies
a) another register
b) another memory location
c) other operand
d) all of the mentioned

96. In a machine instruction format, S-bit is the
a) status bit
b) sign bit
c) sign extension bit
d) none of the mentioned

97. The bit which is used by the ‘REP’ instruction is
a) W-bit
b) S-bit
c) V-bit
d) Z-bit

98. If W-bit value is ‘1’ then the operand is of
a) 8 bits
b) 4 bits
c) 16 bits
d) 2 bits

99. The instructions which after execution transfer control to the next instruction in the sequence are called
a) Sequential control flow instructions
b) control transfer instructions
c) Sequential control flow & control transfer instructions
d) none of the mentioned

100. The instructions that transfer the control to some predefined address or the address specified in the instruction are called as
a) sequential control flow instructions
b) control transfer instructions
c) sequential control flow & control transfer instructions
d) none of the mentioned