DEPARTMENT OF ECE

EMBEDDED SYSTEMS

1. What are the essential tight constraint/s related to the design metrics of an embedded system?

a. Ability to fit on a single chip
b. Low power consumption
c. Fast data processing for real-time operations
d. All of the above

2. Which abstraction level undergo the compilation process by converting a sequential program into finite-state machine and register transfers while designing an embedded system?

a. System
b. Behaviour
c. RT
d. Logic

3. Which characteristics of an embedded system exhibit the responsiveness to the assortments or variations in system's environment by computing specific results for real-time applications without any kind of postponement ?

a. Single-functioned Characteristic
b. Tightly-constraint Characteristics
c. Reactive & Real time Characteristics
d. All of the above

4. Which development tool / program has the potential to allocate the specific addresses so as to load the object code into memory?

a. Loader
b. Locator
c. Library
d. Linker

5. The assembler list file generated by an assembler mainly includes _____

a. binary codes
b. assembly language statements
c. offset for each instruction
d. all of the above

6. Which kind of assembler do not generate the programs in similar language as that used by micro-controllers by developing the program in high-level languages making them as machine independent?

a. Macro Assembler
b. Cross Assembler
c. Meta Assembler
d. All of the above

7. What kind of address/es is /are usually assigned to program by the linker adopted in an execution of assembler?

a. Absolute Address
b. Relative Address starting from unity
c. Relative Addresss starting from zero
d. None of the above

8. What are the major form of functionalities associated to high-level language compilers?

a. Generation of an application program
b. Conversion of generated code from higher level language to machine-level language
c. Both a & b
d. None of the above

9. Which development tool can facilitate the creation and modification of source programs in addition to assembly and higher -level languages?

a. Editor
b. Assembler
c. Debugger
d. High-level language Compiler

10. EPROM Programming versions are of greater significance to designers for _____

a. Debugging of hardware prototype
b. Debugging of software prototype
c. Loading the programs in microcontrollers
d. All of the above

11. What is/are the possible way/s of displaying the data by logic analyzer ?

a. Logic state format
b. Hexadecimal & Map format
c. Timing diagram format
d. All of the above

12. Which type of triggering allow the trigger qualifier circuit to compare the input data word with the word programmed by the user in logic analyzer?

a. Triggering from external input
b. Programmable Triggering
c. Both a & b
d. None of the above

13. Which mandatory contents can be visualized by the hexadecimal display format of a logic analyzer?

a. Data Bus
b. Address Bus
c. Both a & b
d. None of the above

14. How many samples can be displayed before and after the trigger respectively if the trigger-pulse is delayed by center-trigger mode to display 1024 bit counts?

a. 512 & 512 samples respectively
b. 512 & 1024 samples respectively
c. 1024 & 512 samples respectively
d. 1024 & 1024 samples respectively

15. It is a characteristic provision of some debuggers to stop the execution after each instruction because_____

a. it facilitates to analyze or vary the contents of memory and register
b. it facilitates to move the break point to a later point
c. it facilitates to rerun the program
d. it facilitates to load the object code program to system memory

16. Which component is replaced by an in-circuit emulator on the development board for testing purposes?

a. RAM
b. I/O Ports
c. Micro-controller IC
d. All of the above

17. It is feasible for an in-circuit emulator to terminate at the middle of the program execution so as to examine the contents of _____

a. memory
b. registers
c. both a & b
d. none of the above

18. Which operations are not feasible to perform by simulator programs in accordance to real time programming?

a. Memory Operations
b. I/ O Operations
c. Register Operations
d. Debugging Operations

19. Deadline-driven constraints so called

A. Reality-time constraints
B. Real-time constraints
C. Real-data constraints
D. None of above

20.Processor must accept and process frame before next frame arrives, typically called

A. Hard real-time systems
B. Real-time constraints
C. Real-data constraints
D. Soft real-time systems

21. An embedded system must have

(a) hard disk
(b) processor and memory
(c) operating system
(d) processor and input-output unit(s).

22. An embedded system hardware can

(a) have microprocessor or microcontroller or single purpose processor
(b) have digital signal processor
(c) one or several microprocessor or microcontroller or digital signal processor or single purpose processors
(d) not have single purpose processor (s).

23. An embedded system has RAM memory

(a) for storing the variables during program run, stack and input or output buffers, for example, for speech or image
(b) for storing all the instructions and data
(c) for storing the programs from external secondary memory
(d) for fetching instructions and data into cache(s).

24. A system might be connected to a number of other devices and systems.

(i) A bus consists of a common set of lines to connect multiple devices, hardware units and systems (ii) A bus is used for communication between two of these at any given instance. (iii) A bus is used for communication between all of these at the same instance (iv) A bus may be serial bus or parallel bus to transfer one bit or multiple data bits at an instance, respectively.

(a) i, ii and iv correct
(b) iii correct
(c) iii and iv correct
(d) all are correct.

25. A system must have an interrupt handling mechanism for executing the interrupt service routines in case of the interrupts from

(a) physical devices
(b) interfaced circuits or systems, software interrupt instructions and software exceptions
(c) physical devices or interfaced circuits or systems
(d) physical devices or interfaced circuits or systems, software interrupt instructions and software exceptions.

26. In a multitasking OS, (i) each process (task) has a distinct process control block (ii) each process (task) has memory allocation of its own (iii) a task has one or more functions or procedures for a specific job. (iv) a task may share the memory (data) with other tasks. (iv) processor may process multiple tasks separately or concurrently (v) each process (task) has a separate stack in memory (vi) a process calls another process, which can call another process, similar to nested call of the functions.

(a) i, ii, iv and vi correct
(b) all are correct except vi
(c) iii, iv and v correct
(d) ii, iii and vi correct.

27. RTOS is used in most embedded systems when the system does

(a) concurrent processing of multiple real time processes
(b) sequential processing of multiple processes when the tasks have real time constraints (c)

real time processing of multiple processes
(d) the concurrent processing of multiple processes, tasks have real time constraints and deadlines, and high priority task preempts low priority task as per the real time constraints.

28. A device driver is software for

(a) opening or connecting or binding or reading or writing or closing or other actions of the device
(b) receiving input or sending outputs from device
(c) access to parallel or serial port by the device
(d) controlling and configuring the device for read and write functions.

29. Device Manager is software (i) for allocating and registering port (in fact, it may be a register or memory) addresses for the various devices at distinctly different addresses (ii)codes for detecting the presence of devices (iii) for initializing these and for testing the devices that are present (iv) codes for detecting any collision between the device accesses in the system (v) managing driver functions of all physical and virtual devices.

(a) v correct
(b) i, iv and v correct
(c) all correct
(d) all correct except iv.

30. Design metrics are (i) engineering cost (ii) time to market (iii) power dissipation (iv) flexibility (v) system and user safety (vi) performance (vii) prototype development time (viii) maintenance of the system

(a) all
(b) all except v and viii
(c) iii and vi
(d) all except i and ii

31. Total power dissipation reduced by (i) reducing operating voltages, (ii) operating at lower clock frequency if processes meet the deadlines (iii) use of wait and stop instructions when system is inactive or idle (iv) use of cache disabling instructions (v) optimizing the amount and type of hardware required for the system

(a) all except v
(b) i, ii and iii
(c) all except iv
(d) all

32. Besides the main microcontroller in digital camera, the following processors are used in digital camera to enable taking pictures with higher resolution of 4 or 6 M Pixel within required time interval

(a) single purpose processors ─CCD signal processor, CODEC and pixel display processor
(b) single purpose processors─ graphic and display processors
(c) DSPs
(d) embedded processors

33. Sophisticated embedded systems development requires

(a) IPs and several ASIPs,
(b) IPs and several ASIPs, and hardware-software co-design
(c) multi-core processors
(d) system on chip with large memory

34. Cache (i) is a fast *read and write* on-chip memory for the processor execution unit (ii) stores instructions and data fetched in advance from ROM or RAM for use of execution unit and for data write back for RAM (iii) has advantage that processor execution unit does not have to wait for instruction and data from external buses and also does faster write back of data meant for RAM (iv) use is must in embedded system with large memory requirements (v) has lower power dissipation compared to RAM

(a) i, ii, iii and iv
(b) i, iii, iv and v
(c) i, ii, iii and v
(d) i, ii and iii

35. A communication protocol specifies (i) the ways of communication of signals on the bus (ii) ways of arbitration when several devices need to communicate through the bus or the ways of polling from the devices need of the bus at an instance (iii) memory requirement during communication (iv) minimum rate of data transfer during communication (v) interrupt service mechanism

(a) i, ii, iii and iv
(b) i, iii, iv and v
(c) i and ii
(d) i, ii and iii